

Migration from W5100 to W5200

This application note describes what designers and programmers should consider when migrating from W5100 to W5200. For additional information about the W5200, please refer to the W5200 datasheet. This document contains the following topics:

- Section 1, "Comparison"
- Section 2, "Hardware Considerations"
- Section 3, "Software Considerations"
- Section 4, "References"

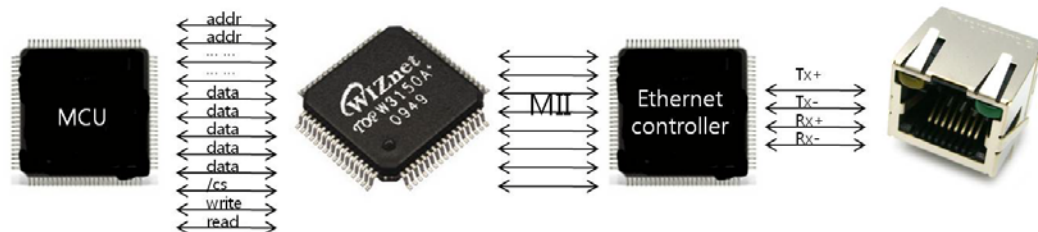
1. Comparison

1.1 Advantages and Challenges of Migration

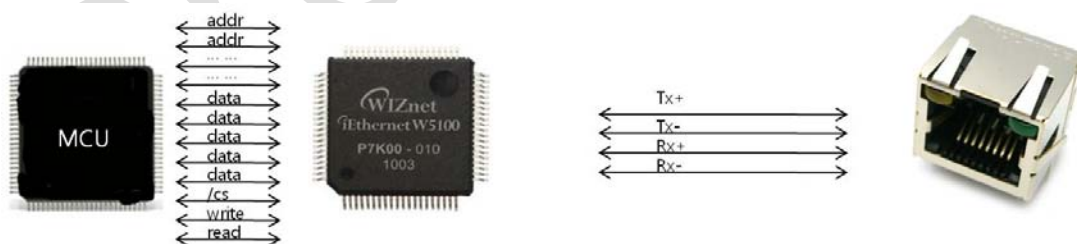
This section highlights the various advantages and challenges involved when migrating from W5100 to the W5200.

The W5200 provides a higher level of performance while maintaining many characteristics of the W5100's architecture. Following is a list of the advantages of migrating to the W5200.

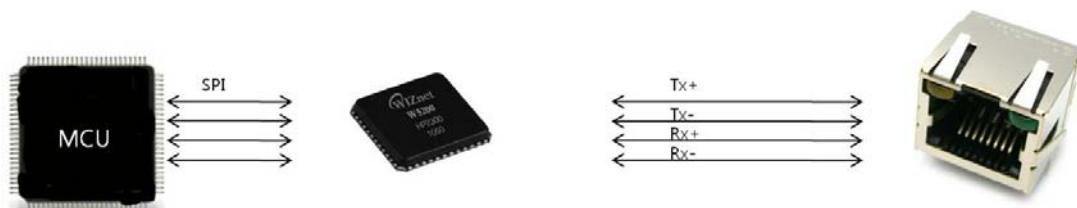
- Cost effective.
- Easy to use
 - W3150A+



■ W5100



■ W5200



- Space reduction
- More H/W sockets available
- Supports power down mode
- Supports byte and burst read/write operation
- Embedded PHY status register made checking LINK status easy

Following is a list of differences that may present challenges in migrating from the W5100 to the W5200:

- Different package and pinout. See Section 2, “ Hardware Considerations ” for information on addressing these differences.
- Different SPI command format, so driver is not fully compatible.

1.2 Summary and Feature Comparison tables

Table 1 includes information comparing some of the features of W5100 and W5200.

Table 1. W5100 and W5200 Comparison

		W5100	W5200
H/W	Core	H/W IPv4	
	Voltage	3.3v	
	H/W Reset	Low active	
	Ethernet core clock	25Mhz	
	Package	Small 80-pin LQFP	Small 48-pin QFN
	MCU bus I/F	Direct / Indirect / SPI	SPI
	Max SPI clock	4MHz	80MHz
	SPI read/write operation	byte	Byte and burst
	Tx/Rx memory	16k byte	32k byte
	Socket number	4	8
Function	TCP/IP protocol	TCP.UDP.IP.ARP.ICMP.MAC. IGMP(UDP Multicasting) PPPOE(ADSL) Ethernet (PHY)	
	SEND_OK interrupt	Support	
	No delayed ACK	Support in TCP mode	
	Interrupt register clear	By writing "1"	
	RD/WR Pointer register	2 byte registers	
	Receive Data Size / Free Tx Buffer Size register	Support	
	Keep alive command	Support	
	Direct send command without ARP	Support	

2. H/W consideration

2.1 Voltage

Both models are 3.3v device.

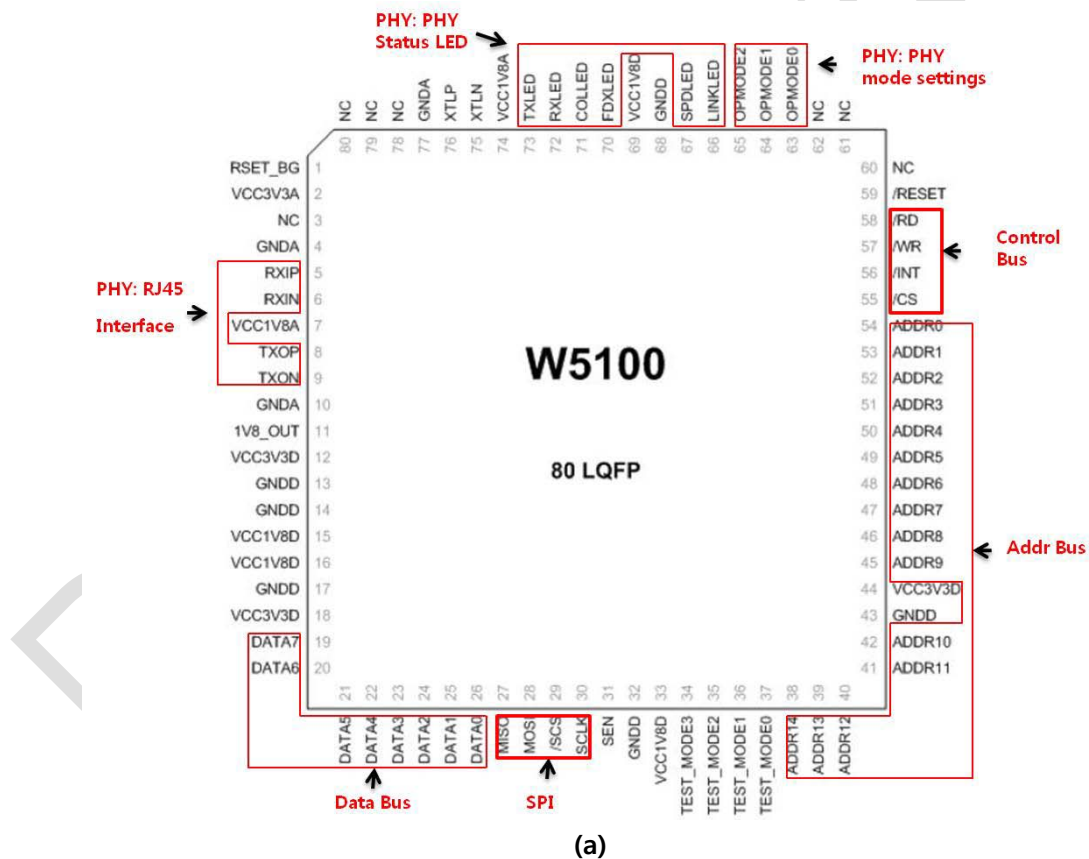
2.2 Package and Pinout

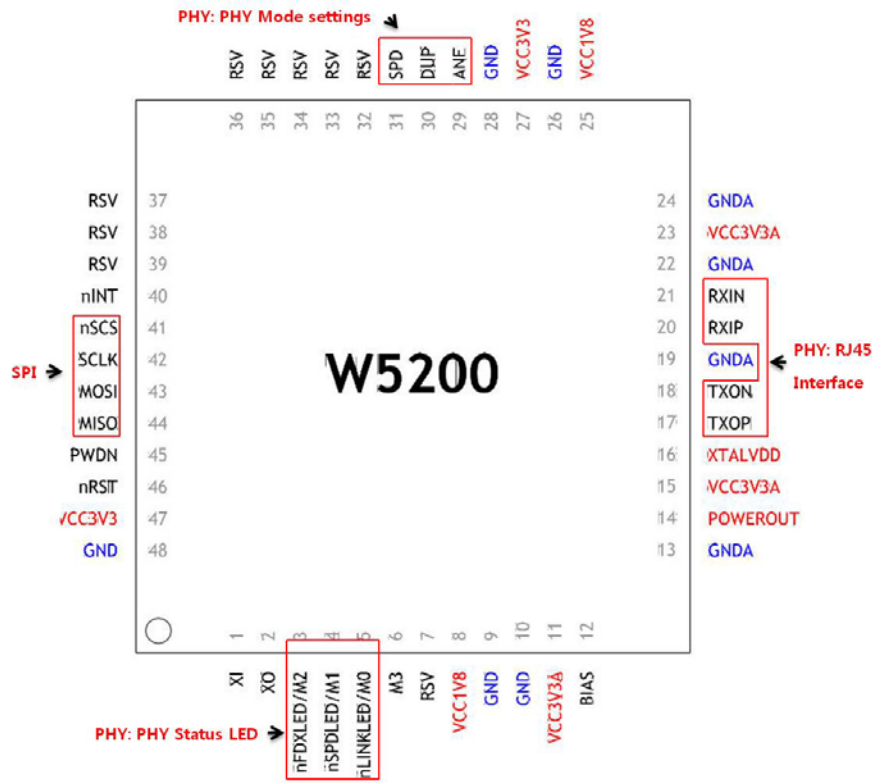
a) The pinout has a huge difference. One main factor made this difference.

- As Direct and Indirect bus is removed in W5200, SPI is the only way used to interface host MCU.

b) Pinout considerations:

There are two parts that users should note when migrate W5100 to W5200. They are MCU interface and PHY interface. MCU interface consists of Control bus, Address bus, Data bus and SPI. PHY interface consists of PHY mode setting interface, RJ45 and PHY Status LED. As long as these parts were fully understood, users could easily do the H/W migration from W5100 to W5200.





(b)

Fig. 1 Pinout considerations when migrate W5100 to W5200

- c) In our website, users can find reference schematic of W5100 and W5200. By this way, more H/W related information can be found so that the H/W migration from W5100 to W5200 can be done very soon.

2.3 Host MCU interface

W5200 is designed for space reduction. Thus, in terms of host MCU interface, Direct and Indirect interface is removed. SPI is the only way used to interface host MCU. In order to improve the performance, W5200 supports maximum 80MHz SPI clock source and burst read/write operation. Thus, if you were using Direct or Indirect way to communicate with your host MCU, when migrate W5100 to W5200 you must use SPI this new solution. Of course, your host MCU must support SPI master.

2.4 Register write/read timing

The two chipsets have different SPI command formats. For example, W5200 not only supports byte read/write operation, but also supports burst read/write operation. In this case, their write/read timing definitely has a huge difference.

When migrating from W5100 to W5200, users must carefully follow W5200's timing. For more information, please refer to W5200's datasheet: 6.3 Process using general SPI master device & 7.4.3 SPI Timing.

2.5 Tx/Rx memory

W5200 supports 32KB Tx/Rx memory. Thus, do not consider the memory limitation when migrating from W5100 to W5200.

2.6 Registers

2.6.1 Register Map

Although both W5100 and W5200 consist of Common register, Socket register, and Tx/Rx memory, W5200 supports larger size Tx/Rx memory than W5100 and a few new registers were designed in it. Thus, the register map is not the same.

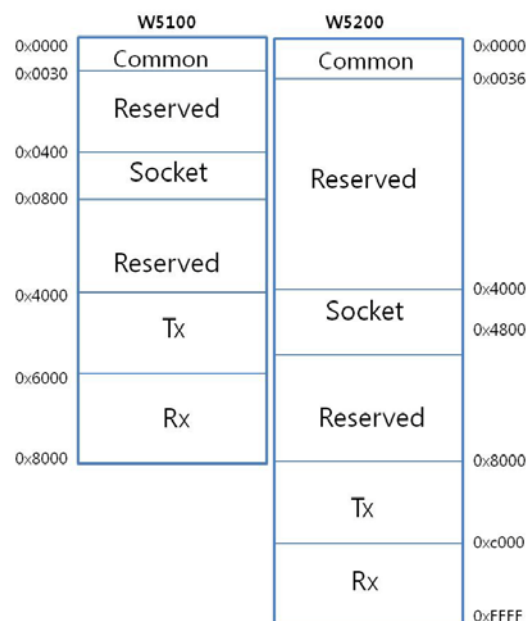


Figure 2. The register map of W5100 and W5200

2.6.2 Registers comparison

Most registers in W5200 is compatible with those in W5100, even with the same offset. Only few registers were newly designed in W5200.

Common registers:

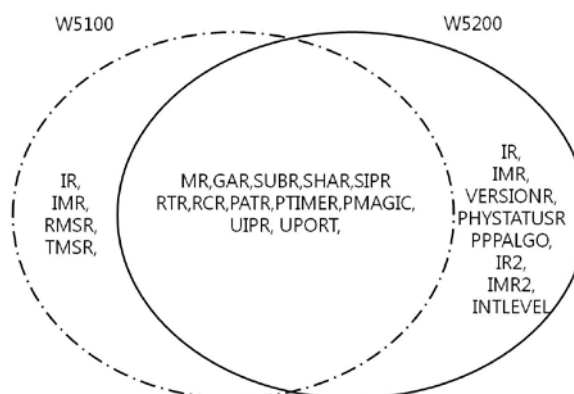


Figure 3. Common registers comparison

Description:

IR

Table.2 IR comparison between W5100 and W5200

	W5100	W5200
Bit7	CONFLICT	
Bit6	UNREACH	RESERVED
Bit5	PPPoE	PPPoE
Bit4	RESERVED	Reserved
Bit3	S3_INT	Reserved
Bit2	S2_INT	Reserved
Bit1	S1_INT	Reserved
Bit0	S0_INT	Reserved

W5200 supports 8 independent h/w sockets which is 4 more socket than W5100. Thus, in order to accommodate the whole 8 sockets, a register called IR2 is newly designed in W5200.

IR2

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
S7_INT	S6_INT	S5_INT	S4_INT	S3_INT	S2_INT	S1_INT	S0_INT

INTLEVEL

This register also is the newly designed register in W5200. It seems like a delay timer which allows W5200 to not that timely response TCP/IP core's interrupt request. For more information, refer to W5200 datasheet.

PHYSTATUS

This register is new register too. It indicates the PHY status of W5200. LINK status seems the most important PHY status. Before W5200, users tried many ways to check the LINK status, but effect was not good. Currently, by using PHYSTATUS, users can easily solve this problem.

For example: By using PHYSTATUS, user can easily know whether cable is connected or plugged out by someone.

Socket registers:

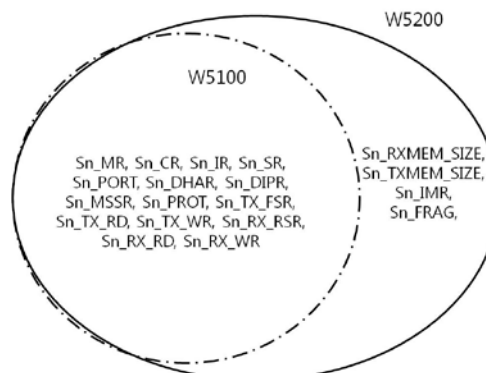


Figure 4. Socket registers comparison

Migration from W5100 to W5200

3. S/W consideration

3.1 Software library

S/W migration refers to driver migration. Essentially, the function of WIZnet driver is to use API to read and write WIZnet chip's registers. Before W5200, users have three options:

- Read/write registers by Direct interface
- Read/write registers by Indirect interface
- Read/write registers by SPI/I2C

Now, only SPI is available. In addition, as the SPI command format of W5100 and W5200 is different, their SPI-based driver is not fully compatible. In order to solve this problem, the easiest way is to find sample code and port it to your application. Our website provides users with many sample code, such as TCP/UDP sample code, Telnet sample code and so on, please refer to them.

4. Reference

W5100 sample code and reference schematic can be found through below link:

<http://www.wiznet.co.kr/W5100/download>

W5200 sample code and reference schematic can be found through below link:

<http://www.wiznet.co.kr/W5200/download>